CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices; and

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; ~~and~~

~~wherein~~ said structurable hardware unit having direct connections and configurable data paths and data linkage paths between devices to be connected by said structurable hardware unit ~~is configured to evaluate and process data and/or signals received thereby~~.

Claim 2 (original). The program-controlled unit according to claim 1, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

Claim 3 (original). The program-controlled unit according to claim 1, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

Claim 4 (original). The program-controlled unit according to claim 3, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

Claim 5 (original). The program-controlled unit according to claim 1, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

Claim 6 (currently amended). The program-controlled unit according to claim 1, wherein ~~said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal,~~ said logic block unit ~~enabling~~ enables devices to be connected via said structurable hardware unit to cooperate as desired.

Claim 7 (original). The program-controlled unit according to claim 6, wherein said clock generation unit and said logic block unit each contain configurable elements.

Claim 8 (original). The program-controlled unit according to claim 6, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 9 (original). The program-controlled unit according to claim 6, wherein the logic block unit is formed at least in

part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 10 (original). The program-controlled unit according to claim 6, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

Claim 11 (original). The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

Claim 12 (original). The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as a state machine for central sequence control.

Claim 13 (original). The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

Claim 14 (original). The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as an

instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

Claim 15 (original). The program-controlled unit according to claim 1, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

Claim 16 (original). The program-controlled unit according to claim 1, wherein said structurable hardware unit is reversibly configurable.

Claim 17 (original). The program-controlled unit according to claim 16, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

Claim 18 (original). The program-controlled unit according to claim 1, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

Claim 19 (original). The program-controlled unit according to claim 1, wherein a configuration of said structurable hardware unit is enabled at any time.

Claim 20 (currently amended). A program-controlled unit, comprising:

an intelligent core having an instruction pipeline and processing instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices; and

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; ~~and~~

~~wherein said structurable hardware unit is configured to inject instructions into said instruction pipeline of said~~

~~intelligent core,~~ said structurable hardware unit including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal.

Claim 21 (original). The program-controlled unit according to claim 20, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

Claim 22 (original). The program-controlled unit according to claim 20, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

Claim 23 (original). The program-controlled unit according to claim 22, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

Claim 24 (original). The program-controlled unit according to claim 20, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

Claim 25 (currently amended). The program-controlled unit according to claim 20, wherein ~~said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal,~~ said logic block unit ~~enabling~~ enables devices to be connected via said structurable hardware unit to cooperate as desired.

Claim 26 (original). The program-controlled unit according to claim 25, wherein said clock generation unit and said logic block unit each contain configurable elements.

Claim 27 (original). The program-controlled unit according to claim 25, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 28 (original). The program-controlled unit according to claim 25, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF

logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 29 (original). The program-controlled unit according to claim 25, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

Claim 30 (original). The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

Claim 31 (original). The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as a state machine for central sequence control.

Claim 32 (original). The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

Claim 33 (original). The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as an

instruction injection device for injecting instructions into said instruction pipeline of said intelligent core.

Claim 34 (original). The program-controlled unit according to claim 20, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

Claim 35 (original). The program-controlled unit according to claim 20, wherein said structurable hardware unit is reversibly configurable.

Claim 36 (original). The program-controlled unit according to claim 35, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

Claim 37 (original). The program-controlled unit according to claim 20, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

Claim 38 (original). The program-controlled unit according to claim 20, wherein a configuration of said structurable hardware unit is enabled at any time.

Claim 39 (withdrawn). A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to generate and to output signals selected from the group consisting of interrupt requests and event-signaling messages.

Claim 40 (withdrawn). The program-controlled unit according to claim 39, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

Claim 41 (withdrawn). The program-controlled unit according to claim 39, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

Claim 42 (withdrawn). The program-controlled unit according to claim 41, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

Claim 43 (withdrawn). The program-controlled unit according to claim 39, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

Claim 44 (withdrawn). The program-controlled unit according to claim 39, wherein said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

Claim 45 (withdrawn). The program-controlled unit according to claim 44, wherein said clock generation unit and said logic block unit each contain configurable elements.

Claim 46 (withdrawn). The program-controlled unit according to claim 44, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 47 (withdrawn). The program-controlled unit according to claim 44, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 48 (withdrawn). The program-controlled unit according to claim 44, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

Claim 49 (withdrawn). The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

Claim 50 (withdrawn). The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as a state machine for central sequence control.

Claim 51 (withdrawn). The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

Claim 52 (withdrawn). The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

Claim 53 (withdrawn). The program-controlled unit according to claim 39, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

Claim 54 (withdrawn). The program-controlled unit according to claim 39, wherein said structurable hardware unit is reversibly configurable.

Claim 55 (withdrawn). The program-controlled unit according to claim 54, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

Claim 56 (withdrawn). The program-controlled unit according to claim 39, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

Claim 57 (withdrawn). The program-controlled unit according to claim 39, wherein a configuration of said structurable hardware unit is enabled at any time.

Claim 58 (withdrawn). A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to selectively react to interrupt requests or other event-signaling messages from devices connected thereto and prevent the interrupt requests or the event-signaling messages from being forwarded.

Claim 59 (withdrawn). The program-controlled unit according to claim 58, wherein said structurable hardware unit is

disposed in circuit terms between said intelligent core and said plurality of units.

Claim 60 (withdrawn). The program-controlled unit according to claim 58, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

Claim 61 (withdrawn). The program-controlled unit according to claim 60, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

Claim 62 (withdrawn). The program-controlled unit according to claim 58, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

Claim 63 (withdrawn). The program-controlled unit according to claim 58, wherein said structurable hardware unit comprises

a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

Claim 64 (withdrawn). The program-controlled unit according to claim 63, wherein said clock generation unit and said logic block unit each contain configurable elements.

Claim 65 (withdrawn). The program-controlled unit according to claim 63, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 66 (withdrawn). The program-controlled unit according to claim 63, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

Claim 67 (withdrawn). The program-controlled unit according to claim 63, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

Claim 68 (withdrawn). The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

Claim 69 (withdrawn). The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as a state machine for central sequence control.

Claim 70 (withdrawn). The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

Claim 71 (withdrawn). The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

Claim 72 (withdrawn). The program-controlled unit according to claim 58, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

Claim 73 (withdrawn). The program-controlled unit according to claim 58, wherein said structurable hardware unit is reversibly configurable.

Claim 74 (withdrawn). The program-controlled unit according to claim 73, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

Claim 75 (withdrawn). The program-controlled unit according to claim 58, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

Claim 76 (withdrawn). The program-controlled unit according to claim 58, wherein a configuration of said structurable hardware unit is enabled at any time.

Claim 77 (new). The program-controlled unit according to claim 1, wherein said structurable hardware unit is configured for access to said memory devices independently of said intelligent core and for evaluating and processing data and signals received thereby, said structurable hardware unit

including a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal.

Claim 78 (new). The program-controlled unit according to claim 20, wherein said structurable hardware unit has direct connections and configurable data paths and data linkage paths between devices to be connected by said structurable hardware unit, and said structurable hardware unit is configured for access to said memory devices independently of said intelligent core and for injecting instructions into said instruction pipeline of said intelligent core.